

GP/2816



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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Leonard Forbes et al.

Title: DRAM SENSE AMPLIFIER FOR LOW VOLTAGES

Docket No.: 303.586US1

Filed: May 26, 1999

Examiner: Anh-Quan Tra

Serial No.: 09/320,421

Due Date: May 15, 2002

Group Art Unit: 2816

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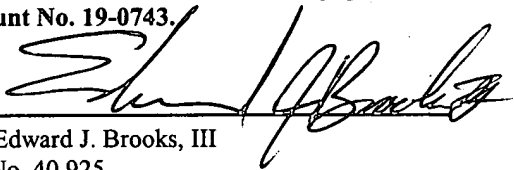
Commissioner for Patents
Washington, D.C. 20231

We are transmitting herewith the following attached items (as indicated with an "X"):

- ☒ A return postcard.
- ☒ An Amendment and Response Under 37 CFR 1.111 (5 Pages).

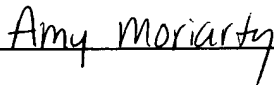
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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on this 27 day of March, 2002.

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#17/Response

S/N 09/320,421

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Leonard Forbes et al.

Examiner: Anh-Quan Tra

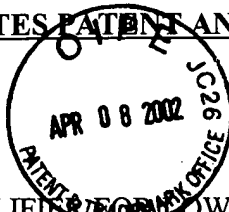
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Title: DRAM SENSE AMPLIFIER FOR LOW VOLTAGES



4/17/02

Schmitt

AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111

Commissioner for Patents
Washington, D.C. 20231

Applicant has reviewed the Office Action mailed on February 15, 2002. Please amend the above-identified patent application as follows.

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REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on February 15, 2002, and the references cited therewith.

No claims are amended, no claims are canceled, and no claims are added; as a result, claims 10, 11, 13-18, 20-24, 26-38, and 40-45 are now pending in this application.

§103 Rejection of the Claims

Claims 10, 11, 13-18, 20-24, 26, 27, 29-38, and 44 and 45 were rejected under 35 USC § 103(a) as being unpatentable over Austin (U.S. 5,982,690) in view of Chung (U.S. 5,442,209).

The rejection states in relevant part:

Figure 1D (Austin) shows all limitations of the claim (claim 10) except for the pair of MOSFETs is a dual gated MOSFET. However, Chung teaches in figure 1 a MOS transistor comprising a single drain, a single source and plurality of gates. The advantage of Chung's MOSFET is the chip area can be reduced in device fabrication. Therefore, it would have been obvious to one having ordinary skill in the art to make Austin's pair MOSFET (153 and 154) as a transistor having a single drain, single source, and two gates (dual gated MOSFET) for the purpose of saving space.

These remarks by the examiner seem to indicate that the purpose of saving space is a primary motivation in the Applicant's case. This alone does not provide a motivation to combine the Chung reference with the Austin reference. The Chung reference appears to be